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FORMAL SPECIFICATION OF ON-CHIP COMMUNICATIONS: STATE OF THE ART

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ABSTRACT

Nowadays Systems-on-Chip (SoCs) have evolved considerably in term of performances, reliability and integration capacity that has induced the growth of the number of cores (IPs) in a same chip. In fact, multiplying the core's number of the same chip has conducted to internal signals communication problems and conventional buses were not able to manage too many cores with too many signals. To resolve this problem of intra-communication between the elements of a same chip, a new concept has been introduced which is a direct result of the complexity of recent and future SoCs, it is the Network on Chips (NoC). In this poster we present a state of the art on few formal methods that improve the specification of communication in Network on Chips according to their on-chip communication, the problems they address and the different languages they use.

Keywords— network on chip, formal specification, formal methods, wormhole switching, routing, communication.

1. INTRODUCTION

The NoC paradigm has been herald as the solution to the communication limitation that System-On-Chip (SoC) poses [1]. NOC was important because it allowed design engineers to follow technology advancements and so, integrating many cores at the same chip by overcoming the intra-communication problems [2]. Generally, NOC are evaluated with respect to their performance parameters, such as energy consumption, area, communication bandwidth, throughput and latency [3]. NOC exploits a layered approach to ensure data transfer between IPs, which can be processors, memories, dedicated blocks, etc. Figure 1 present the elements of a common NOC: Network Interfaces (NI), Physical Links (PL) and Routers (R) [4].

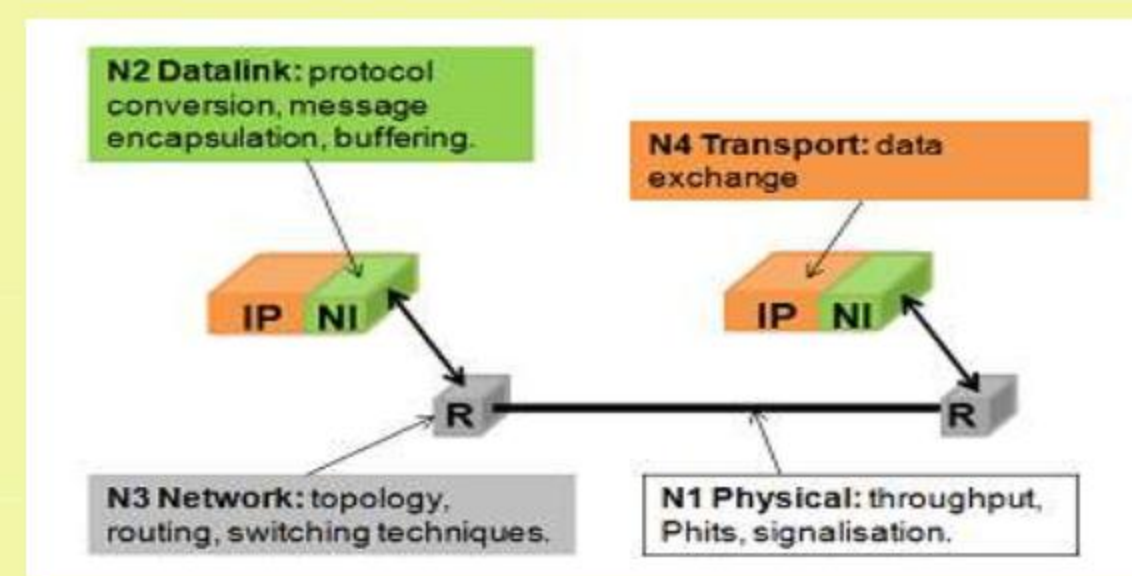


Figure 1. Elements of common NOC.

In this poster, we present a state of the art on formal methods that improve the specification of communication in Network on

Chips. We introduce some concepts of NOCs and define the communication in NOCs. Next, we present the some works on formal specification of the communication inside NOCs [5].

2. COMMUNICATION IN NOC

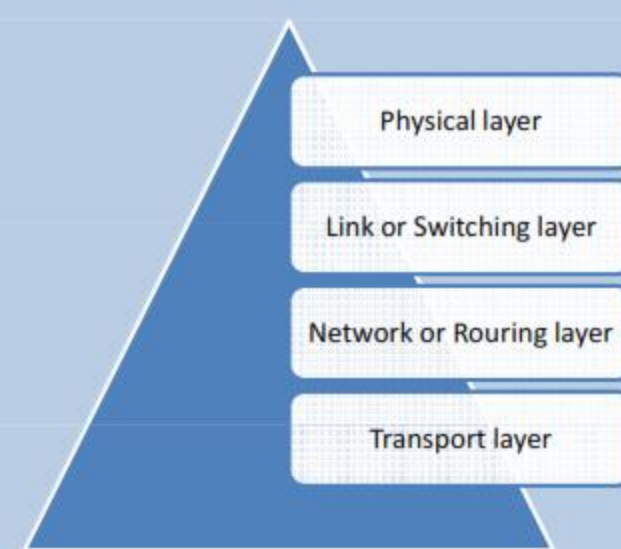


Figure 2. NOC Layers.

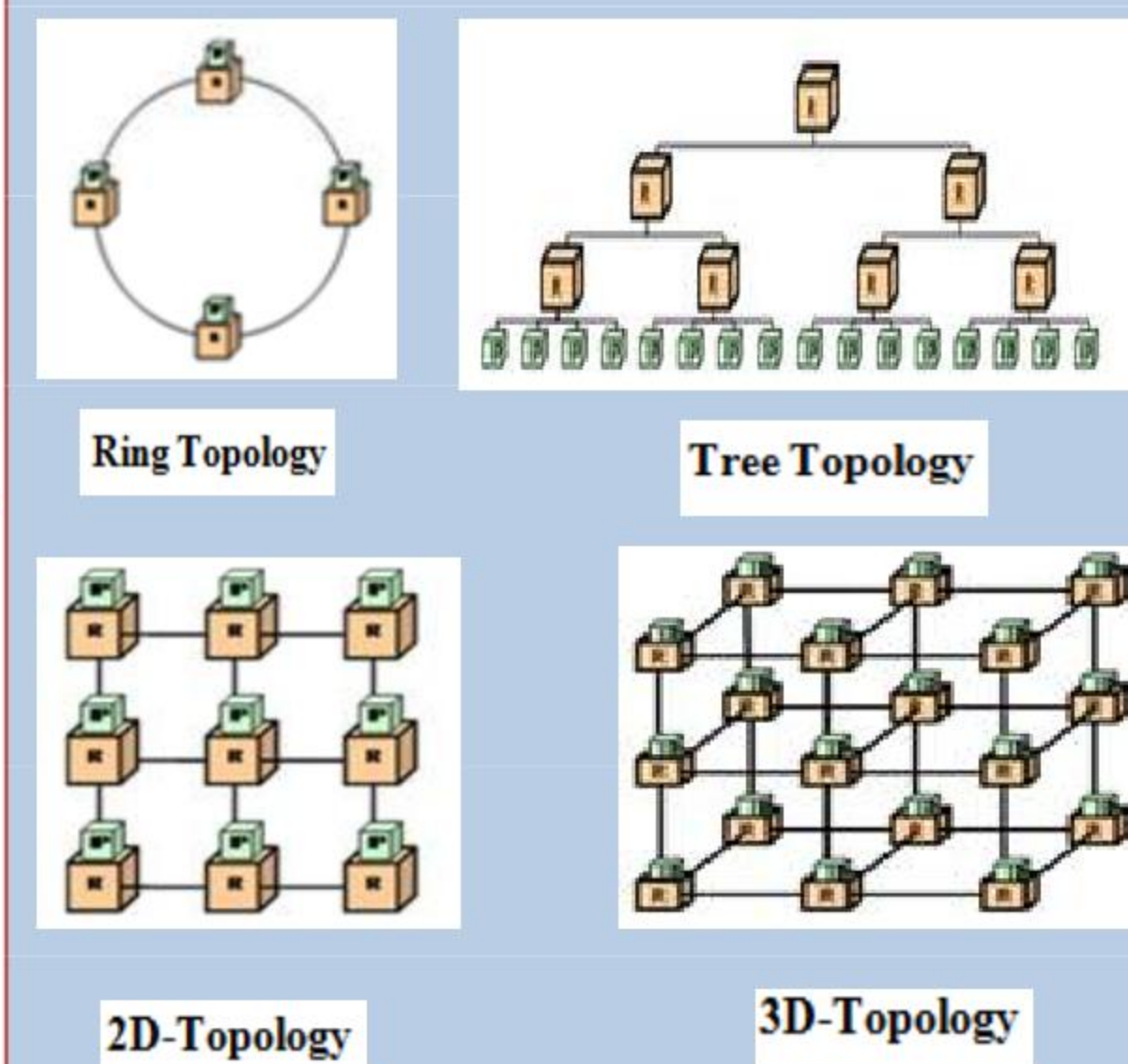


Figure 3. NOC Topologies.

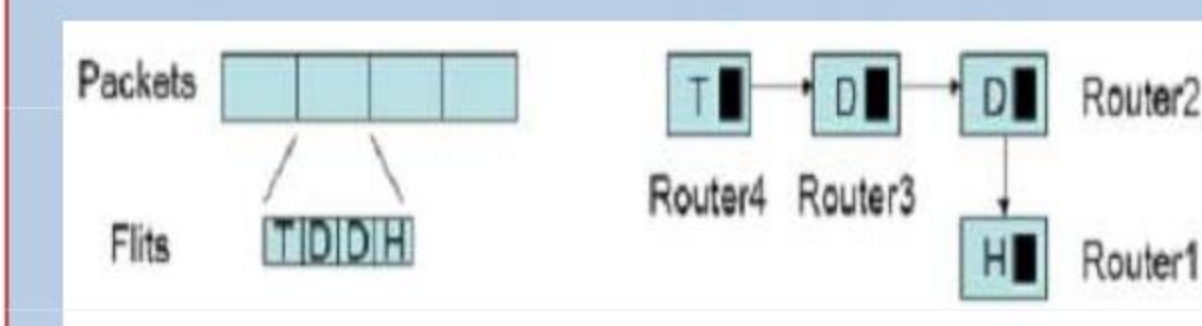


Figure 4. Wormhole Switching.

3. FORMAL METHODS

The application domain of SOC spans from home use electronics to large safety critical control and data transfer systems. One of the appropriate approaches for specifying reliable SOC, modeling the on-chip communication, as well as verifying their design is provided by formal methods [6]. The main advantage of formal methods use is the possibility to prove all cases by extending the test space. As formal languages have mathematical foundation, it is possible to formally verify essential design properties [7].

4. RELATED WORKS

Specification of NoC models may be classified based on the specification methodology, as shown in Table 1.

Reference	Formal Method	NOC	Routing Algorithm	Switching	Success	Failed
[7]	Z notation	2D Mesh	-	-	+	-
[8]	Concurrent Haskell	Spinnaker	-	-	+	-
[9]	ACL2 Logic	Octagon	Shortest Path	Circuit Switching	+	-
[10]	ACL2 Sedan	HERMES	XY routing	Wormhole	+	-
[11]	SDL	KITH-VTT	Dynamic	-	+	-
[12]	PVS	ETHEREAL	-	packet switch	+	-
[13]	Promela	PNOC	-	Circuit Switching	+	-

Table 1. Comparison of formal specification methods of NOC.

5. CONCLUSION

Several formal methods for specification and verification of NoC can be found in the literature. By suggestion and comparison of some techniques, the results can help designers to have a more realistic model and a more accurate analysis.

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