Machine Structure 2 Examination

Duration: 90 minutes

For exercise 3, question 2 and 4, answer directly on the provided exam document.

Exercise 1 (7pt)

1- Provide the logical expressions for the outputs Si, Ii, Ei. (2 pt)

Xi	Yi	Si	Ii	Ei
0	0	0	0	1
1	0	1	0	0
0	1	0	1	0
1	1	0	0	1

$Si = Xi \cdot \bar{Y}i$

$Ii = \bar{X}i \cdot Yi$

$Ei = xi \cdot yi + \bar{X}i \cdot \bar{Y}i = \overline{Xi \oplus Yi}$

2- Provide logical expressions for the outputs S, I, and E based on the outputs Si, Ii, Ei with i=0, 1, 2 from the 1-bit comparator. (3pt)

To compare two, 3-bit binary, numbers we need to compare bit by bit, starting with the most significant bits. If they are equal, proceed to compare the immediately lower significant bits, and so on.

- X>Y if :
x2 > y2 (S2 = 1)
or x2 = y2 (E2 = 1) and x1 > y1 (S1 = 1)
or x2 = y2 (E2 = 1) and x1 = y1 (E1 = 1) and x0 >y0 (S0 = 1)
So : S = S2 + E2.S1 + E2.E1.S0
- X<Y if:
x2 < y2 (I2 = 1)
or x2 = y2 (E2 = 1) and x1 < y1 (I1 = 1)
or x2 = y2 (E2 = 1) and x1 = y1 (E1 = 1) and x0 <y0 (I0 = 1)
So : I = I2 + E2.I1 + E2.E1.I0
- X = Y if :
x2 = y2 (E2 = 1) and x1 = y1 (E1 = 1) and x0 =y0 (S0 = 1)
So : E = E2.E1.E0

E_2	S_2	I_2	E1	S1	I1	E0	S0	I0		E	S	I
0	1	0	x	x	x	x	x	x		0	1	0
1	0	0	0	1	0	x	x	x		0	1	0
1	0	0	1	0	0	0	1	0		0	1	0
0	0	1	x	x	x	x	x	x		0	0	1
1	0	0	0	0	1	x	x	x		0	0	1
1	0	0	1	0	0	0	0	1		0	0	1
1	0	0	1	0	0	1	0	0		1	0	0

3- Provide the truth table and logical expressions for decoding, enabling the transition from the S, I, E code to the 7-segment code. (2pt)

Inputs			Outputs						
S	I	E	a	b	c	d	e	f	g
1	0	0	1	0	1	1	0	1	1
0	1	0	0	0	0	0	1	1	0
0	0	1	1	0	0	1	1	1	1

$a = d = g = \bar{S} + E$
$b = 0$
$c = S$
$e = I + E = \text{Not } S$
$f = S + I + E = 1$

Exercise 2 (5pt)

1- This circuit features **8 inputs** to **a single output** and incorporates **3 address lines** for the 8 input lines, making it **a multiplexer (MUX 8 to 1)**. where: (1.5pt)

- d_0 to d_7: Input lines
- y: Output
- A_0, A_1, A_2: Address lines
- E: Enable input, active at a low level.

2- (1.5 pt)

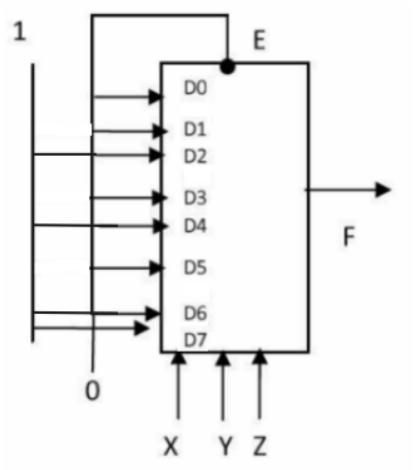
E	A2	A1	A0	Y
1	X	X	X	0
0	0	0	0	d0
0	0	0	1	d1
0	0	1	0	d2
0	0	1	1	d3
0	1	0	0	d4
0	1	0	1	d5
0	1	1	0	d6
0	1	1	1	d7

$$y = \bar{E}[(\overline{A_2}\,\overline{A_1}\,\overline{A_0})d_0 + (\overline{A_2}\,\overline{A_1}A_0)d_1 + (\overline{A_2}A_1\overline{A_0})d_2 + (\overline{A_2}A_1A_0)d_3 + (A_2\overline{A_1}\,\overline{A_0})d_4 + (A_2\overline{A_1}A_0)d_5 + (A_2A_1\overline{A_0})d_6 + (A_2A_1A_0)d_7]$$

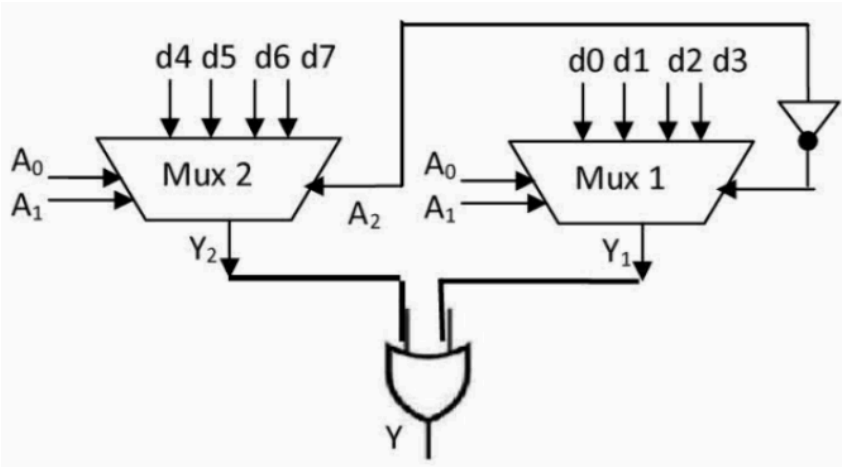
3- (1pt)

F(x,y,z) = Σ(2, 4, 6, 7)

x	y	z	f	di
0	0	0	0	d0 = 0
0	0	1	1	d1 = 0
0	1	0	0	d2 = 1
0	1	1	1	d3 = 0
1	0	0	0	d4 = 1
1	0	1	1	d5 = 0
1	1	0	0	d6 = 1
1	1	1	1	d7 = 1



4- (1pt)



Exercice 3 (8 pts)

We want to create **a modulo 8 asynchronous down counter** using a **JK latch** activated on a **rising edge**.

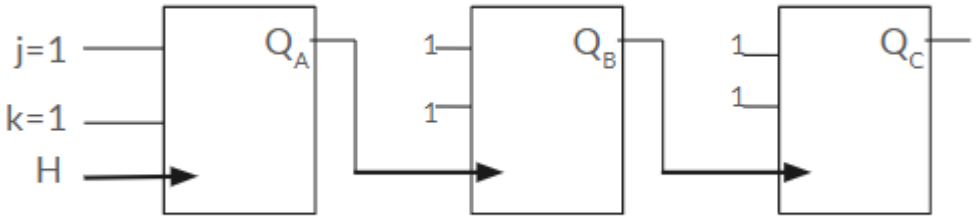
1- Propose a symbolic diagram allowing the creation of this down counter. **(1pt)**

0.25 for nbr of latches (3 latches)

0.25 for setting to 1 the inputs j and k

0.25 for the mode of synchronization

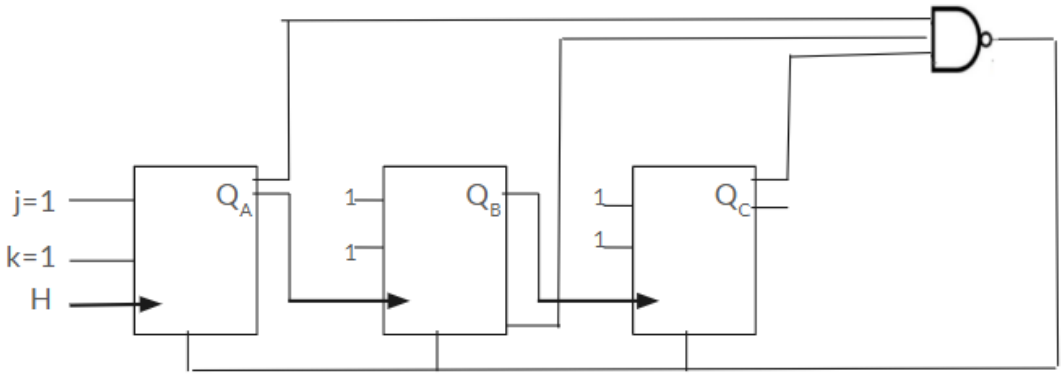
0.25 for wiring : synchronization signal for latch B is the output signal of latch A and the synchronization signal for latch C is the output signal of latch A.



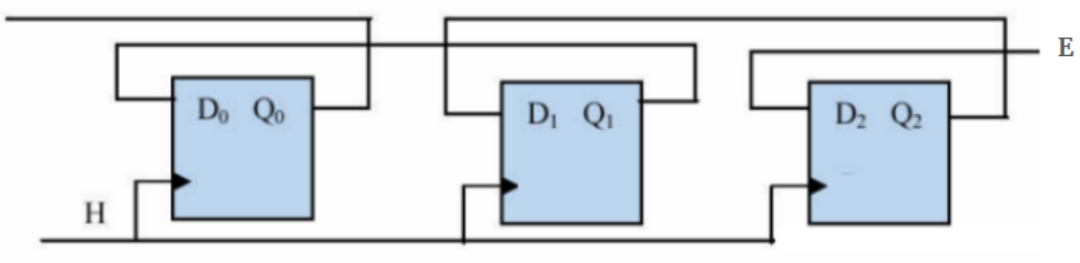
2- Complete the chronogram related to the proposed implementation in question 1.
(0.5 x 4 : 0.5 for each latch + 0.5 for the resulting signal)

3- How can we obtain **a modulo 5 down counter** using the same previous implementation? (draw the new implementation). **(1pt)**

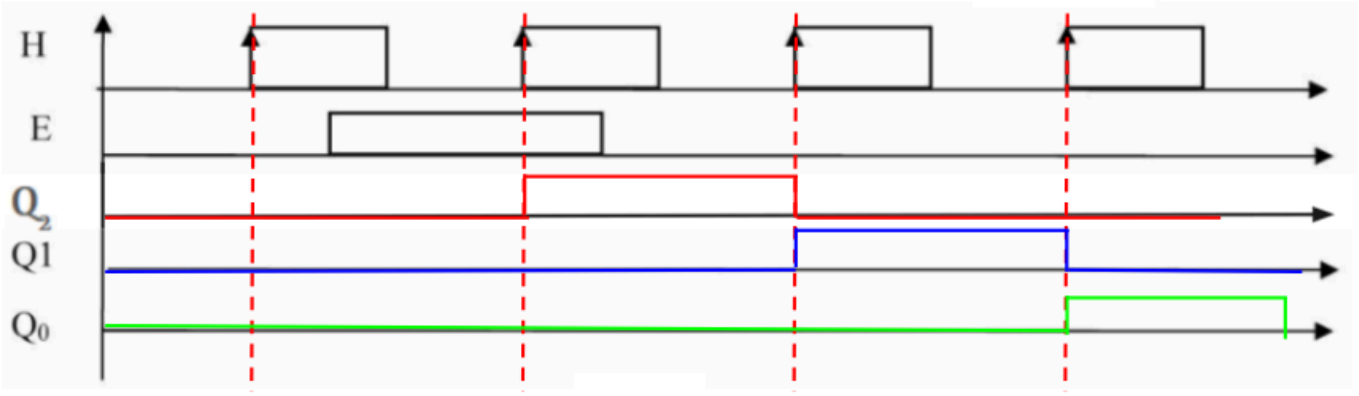
Using NAND gate to stop the counter on 5 (101) value.



Considering the following implementation:

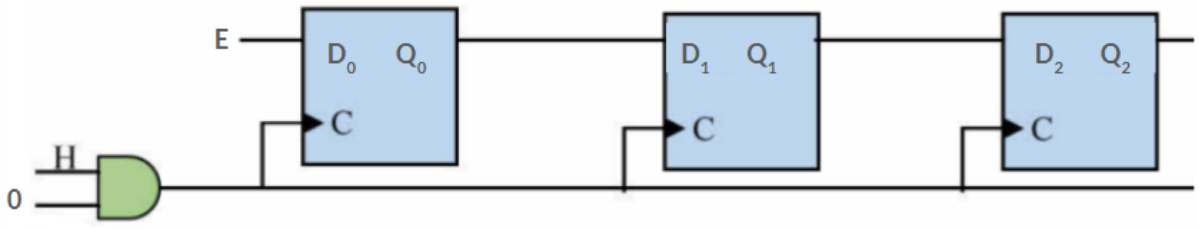


4- Complete the chronogram associated with this circuit and deduce its role. **(0.5 for each latch)**

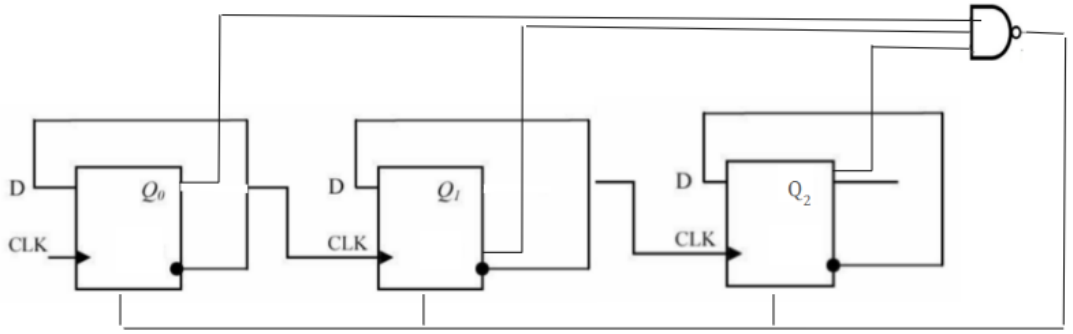


It is a 3-bit left shifting register. (0.5)

5- How can we obtain **a storage register** using the same previous implementation? **(1pt)**



6- How can we obtain **a modulo 5 counter** using the same previous implementation?**(1pt)**



(It existes a seconde solution where the synchronization signal for latch Q1 is the output signal of Q0 by changing the synchronization mode to descending edge mode, and same for latch Q2).