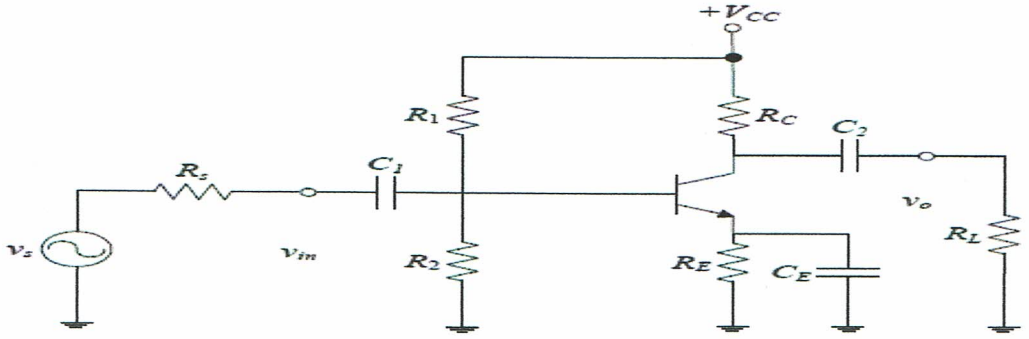
SM Department Oum El Bouaghi University	Analogic Electronics Exam.	1st Year Applied Physics Master

Consider the common-emitter BJT amplifier circuit shown as follow.



Assume that: $VCC = 15$ V, $\beta = 150$, $VBE = 0.7$ V, $RE = 2.7$ kΩ, $RC = 4.7$ kΩ, $R1 = 47$ kΩ, $R2 = 10$ kΩ, $RL = 47$ kΩ, $Rs = 100$ Ω.

Exercise 01 (DC mode)(/6pts)

(a) What are characteristics of DC mode?.

(b) Determine the Q-point.

(c) Sketch the DC load-line.

(d) What is the maximum (peak to peak) output voltage swing available in this amplifier.

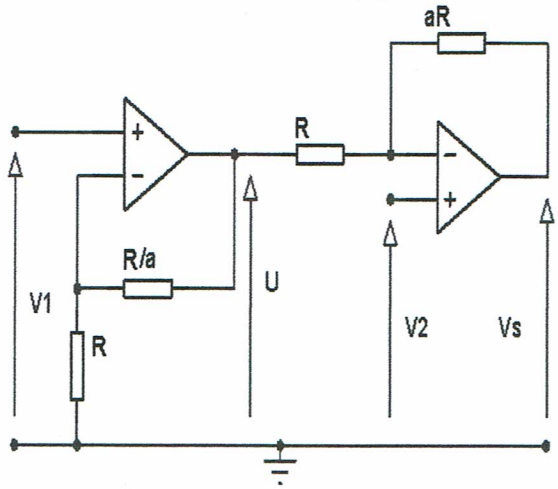
Exercise 02(Ac mode)(/7pts)

(a) What are characteristics of AC mode?.

(b) Draw the AC equivalent circuit (without source neither charge) .

(c) Derive expression for input impedance *Zin and output impedance* , *Zout*

(d) Derive expression for current gain *Ai* and voltage gain *Av*.



Exercise 03(Op Amp)(/7pts)

We give the circuit below

1. How AOPs work.?
2. Determine U as a function of V1 and a.
3. Determine Vs as a function of U and V2.
4. Show that Vs = k(V2 - V1).
5. What value should we give to a so that k =10.5.
6. Give a name to the circuit.

ترجمة عامة للموضوع

أ) ما هي خصائص التشغيل في النمط DC

ب) حدد نقطة الراحة Q للمضخم.

ج) ارسم مستقيم الحمولة السكوني

د) ما هو أقصى تأرجح (من الذروة إلى الذروة) لتوتر الخروج المتاح في هذا المضخم

.التمرين 02

ا) ما هي خصائص التشغيل في النمط AC

ب) ارسم الدارة المكافئة في التيار المتناوب (بدون منبع لا حمولة.(

ج) أعط عبارتي ممانعة الدخول Zin وممانعة الخروج Zout

ج) أعط عبارتي الكسب في التيار Ai والكسب في التوترAv

.التمرين 03

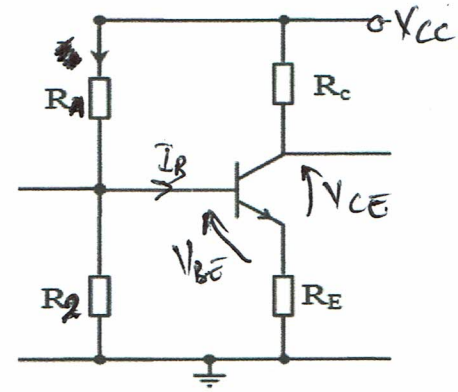
1. .كيف تعمل المضخمات العملية AOPs .؟.
2. حدد عبارةU بدلالة لـ V1 و a
3. حدد عبارة Vs بدلالة لـ U وV2
4. بين أن .Vs = k (V2 - V1)
5. ما هي القيمة التي يجب أن نعطيها لـ a بحيث k = 10.5
6. أعط اسما للدارة.

Detailed Exam Solution

EXERCISE 01(/6pts)

1-a) DC mode is characterized by a constant voltage and current level, meaning that the flow of electrons does not vary over time. In DC equivalent circuit capacitors are replaced by open circuits. 0.5

The dc analysis voltage -divider bias circuit, we have



$V_{TH} = \frac{R_2}{R_2+R_2} V_{CC} = 2.63V$ 0.5

$R_B \approx R_{TH} = \frac{R_2 R_1}{R_2+R_1} = 8.24$ 0.5

$I_B = \frac{V_{TH}-V_{BE}}{R_{TH}+(\beta+1)R_E} = 4.64\mu A$ 0.5

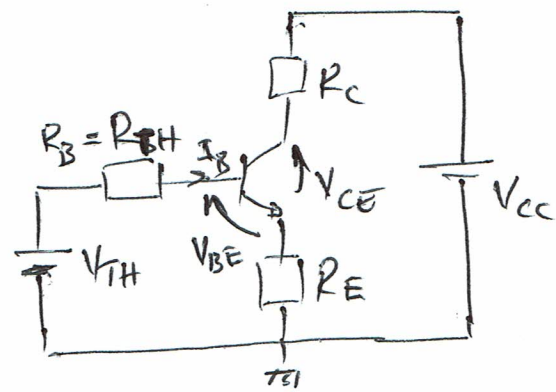
$I_C = \beta I_B = 0.69\ mA$ 0.25

$I_E = (\beta + 1)I_B = 0.70\ mA$ 0.25

$V_E = I_E R_E = 11.72V$ 0.25

$V_C = V_{CC} - I_C R_C = 1.89V$ 0.25

$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 9.84V$ 0.5



1-b) Determination of the Q-point

As $I_B > 0$ and $V_{CE} > 0.2$ V, the transistor is in active region of operation.

The Q-point lies at

ICQ = 0.696 mA

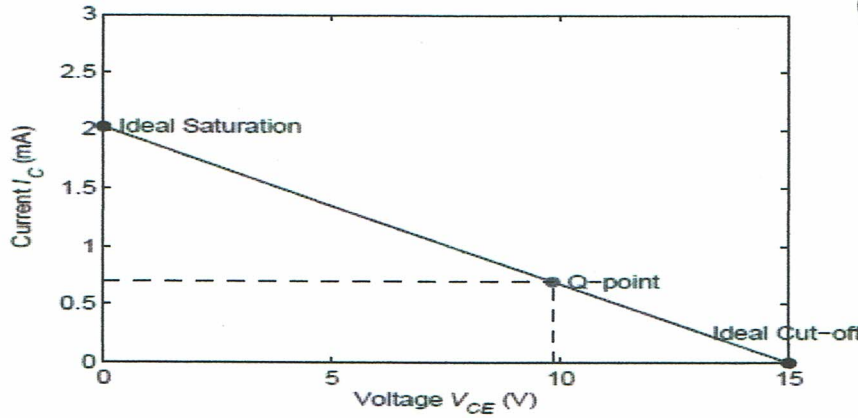
VCEQ = 9.837 V 0.5

2-c) Sketch of the load-line

For ideal saturation $I_{C(SAT)} = \frac{V_{cc}}{R_C+R_E}$; $V_{CE(OFF)} = 15\ V$; $I_{C(SAT)} = 2.027\ V$.

The plot of DC load line is shown in figure below 0.5

0.5



2-d) Maximum peak to peak output voltage swing :

0.5

We see that the Q-point lies closerto cut-off (V_{CE}=15 V) than saturation (V_{CE}=0.2 V).

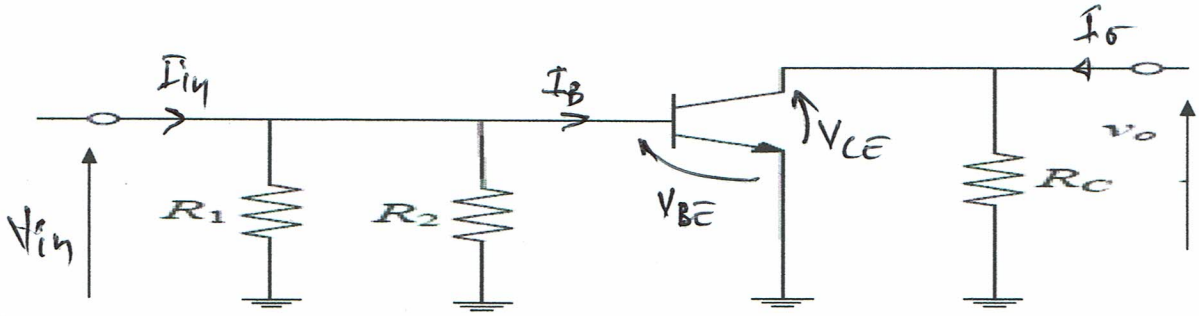
Hense the maximum available peak to peak output voltage swing =2(V_{CC}- V_{CEQ})=10.34 V

EXERCISE 02(/7pts)

2-a) the alternating current (A C) mode is characterized by periodically reverses direction and has a varying voltage and current level. In the AC equivalent circuit the capacitors are replaced by short circuits and Vcc by virtual AC ground.:

1.00

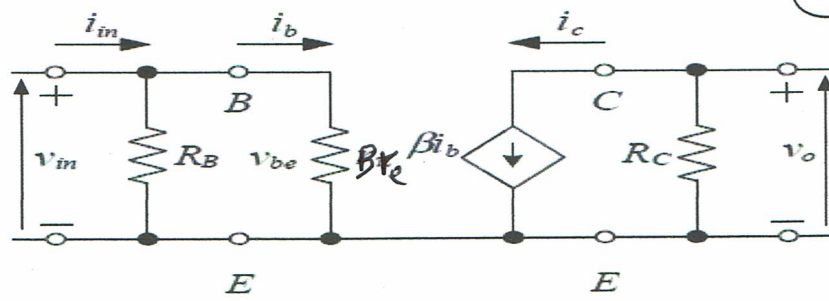
2-b) AC equivalent circuit (without source neither charge)



1.00

Replacing the transistor by its small-signal AC equivalent circuit, we have

1.50



$$r_e = \frac{26mA}{I_{CQ}} = 37.68\Omega$$

0.50

2-c) Expression for input impedance Zin and output impedance , Zout

by definition one can write : $Z_{in} = \frac{v_{in}}{i_{in}}$

from the input loop we have $v_{in} == R_B//(\beta r_e)i_{in}$

1.00

so $Z_{in} = R_B//(\beta r_e)$

From the output loop we have directly : $Z_{out} = \frac{v_o}{i_o} = R_C$

1.00

2-d) Expression for current gain Ai and voltage gain Av.

$A_V = \frac{v_o}{v_{in}}$ by definition

From the output loop $v_o = -\beta i_b R_C$

And from the input loop $v_{in} = \beta r_e i_b \rightarrow i_b = \frac{v_{in}}{\beta r_e}$

0.50

so $v_o = -\beta \frac{v_{in}}{\beta r_e} R_C$

Finally $A_V = \frac{v_o}{v_{in}} = -\frac{R_C}{R_E}$

$$A_i = \frac{i_o}{i_{in}} = \frac{v_o/R_C}{v_{in}/(R_B//(\beta r_e))} = \frac{v_o}{v_{in}} . \frac{(R_B//(\beta r_e)}{R_C}$$

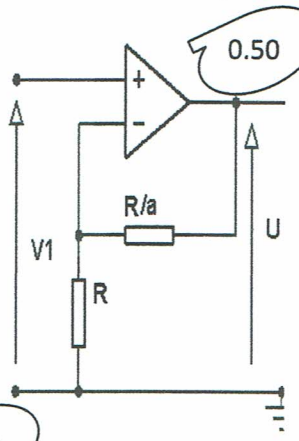
$$A_i = A_v . \frac{(R_B//(\beta r_e)}{R_C}$$

0.50

EXERCICE N°3(/7pts)

3-1) How AOPs work? An operational amplifier is an integrated circuit that can amplify weak electric signals. An operational amplifier has two input pins and one output pin. Its basic role is to amplify and output the voltage difference between the two input pins. 1.50

3-2) Our OP Amp works in linear regime: we assume that $V^+ = V^-$ and $I^+ \cong I^- \cong 0$ 0.50



We can apply the voltage divider to the input loop (u, R/a, R)(see fig 01) to calculate the voltage between the resistor R pins because we have the same current circulates in :

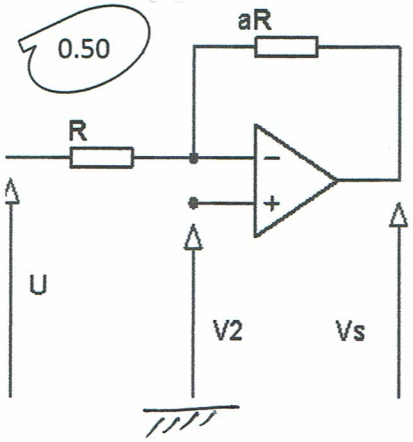
0.50 $V_1 = V^- = \frac{R}{R+R/a}U \rightarrow\rightarrow\rightarrow \boldsymbol{U = \left(1+\frac{1}{a}\right)V_1}$ ....(1) 0.25

3-3) One can apply the KCL law on node A in the output circuit (see fig 02).

0.50 $\frac{V_S-V_2}{aR} = \frac{V_2-U}{R} \rightarrow\rightarrow\rightarrow \boldsymbol{V_S = (1+a)V_2 - aU}$ ..... (2) 0.25

3-4)We replace (1) in (2) , we find $\boldsymbol{V_S = (1+a)(V_2 - V_1) = k(V_2 - V_1)}$ 0.50

3-5) From the last response: $k = (1+a) \rightarrow a = k - 1 \rightarrow\rightarrow \boldsymbol{a = 9.5}$



3-6) The circuit studied is a ***differential amplifier***

0.50